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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TESSERA
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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

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06/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,825	HABA ET AL.	
	Examiner	Art Unit	
	STEVEN J. FULK	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *22-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 30, 2009 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 9, 10, 13-17 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US 5,926,380).

Regarding claims 1 and 9, Kim discloses a method of making mountable devices comprising the steps of: (a) simultaneously mounting terminals of a lead frame incorporating leads and terminals (fig. 4, lead frame 30) to a plurality of spaced-apart caps (fig. 5C, layer 40 covers active region 21 and is considered a cap layer) projecting upwardly from a main surface of at least a portion of a wafer (layer 40 has a thickness, and therefore projects upwardly) having a plurality of individual spaced-apart active areas (fig. 3, 21), each spaced-apart cap covering and protecting a respective spaced-

apart active area of the wafer (layer 40 covers and protects active region 21), the spaced-apart caps defining a plurality of channels between adjacent ones of the active areas and between adjacent ones of the caps (fig. 3, channel formed by contacts 21a); and (b) electrically connecting the terminals mounted on the caps to the wafer by means of leads extending to contacts on the wafer disposed in the channels (fig. 5C, terminals 32 electrically connected to contacts 21a).

Regarding claim 2, the reference discloses the terminal-bearing element (fig. 4, lead frame 30) also includes the leads (32), the step of electrically connecting including bonding the leads to the contacts (fig. 5C, leads 32 bonded to contact 21a through wire bond 50).

Regarding claims 3 and 5, the reference discloses the assembling step is performed so as to position the leads (fig. 5B, 32) at least partially in alignment with the channels (32 is aligned with 21a); wherein the leads are elongated and the assembling step is performed so that at least some of the leads are aligned with channels extending co-directionally with such leads (fig. 5B).

Regarding claim 4, the reference discloses after the assembling step, the leads extend at a level above the contacts (fig. 5C, upper portion of 32 extend above contacts 21a); and wherein the bonding step includes bending the leads downwardly into engagement with the contacts (col. 3, lines 37-42, lead 32 comprises a bend).

Regarding claim 6, the reference discloses wherein the channels include wide channels (fig. 3, 21a) and narrow channels (scribe lines between active areas 21), the

contacts being disposed in the wide channels, the assembling step being performed so as to align the leads with the wide channels (fig. 5B).

Regarding claim 7, the reference discloses the step of severing the wafer in the channels so as to form a plurality of units (col. 4, lines 4-12), each the unit including at least one of the caps, at least one of the terminals and at least one the contact.

Regarding claim 10, the reference discloses the terminal-bearing element to have at least some of the terminals electrically connected to one another prior to the assembling step (fig. 4), the severing step being performed so as to sever at least some connections between the terminals (col. 4, lines 12-16).

Regarding claims 13 and 19, Kim discloses a method of making electronic devices comprising the steps of: (a) simultaneously mounting a plurality of terminals of a terminal-bearing element that includes a lead frame incorporating leads and terminals (fig. 4, lead frame 30) to a structure defining an upper surface (fig. 5C, layer 40) above a main surface of at least a portion of a wafer having a plurality of individual spaced-apart active areas (fig. 3, 21), the structure covering and protecting individual spaced-apart active areas of the wafer (fig. 5C, layer 40 covers an protects active region 21), the structure having depressions extending towards the main surface of the wafer from the upper surface (fig. 5C, depressions where contacts 21a are formed) and contacts in the depressions (21a); and (b) electrically connecting the terminals mounted on the upper surface to the wafer by means of leads extending to the contacts (fig. 5C, terminals 32 electrically connected to contacts 21a) disposed in the depressions.

Regarding claim 14, the reference discloses the terminal-bearing element also includes the leads (fig. 4, lead frame 30 includes leads 32), the step of electrically connecting including bonding the leads to the contacts (fig. 5C, lead 32 is bonded to contact 21a through wire bond 50).

Regarding claim 15, the reference discloses the assembling step is performed so as to position the leads (fig. 5B, 32) at least partially in alignment with the depressions (32 is aligned with depressions containing contact 21a).

Regarding claim 16, the reference discloses after the assembling step, the leads extend at a level above the contacts (fig. 5C, upper portion of 32 extend above contacts 21a); and wherein the bonding step includes bending the leads downwardly into engagement with the contacts (col. 3, lines 37-42, lead 32 comprises a bend).

Regarding claim 17, the reference discloses the step of severing the so as to form a plurality of units (col. 4, lines 4-12).

Regarding claim 20, the reference discloses the terminal-bearing element to have at least some of the terminals electrically connected to one another prior to the assembling step (fig. 4), the severing step being performed so as to sever at least some connections between the terminals (col. 4, lines 12-16).

Regarding claim 21, the reference discloses the structure defining the upper surface includes a plurality of spaced-apart caps (fig. 5C, layer 40 covers active region 21 and is considered a cap layer) defining the depressions as channels extending between adjacent ones of the individual spaced-apart active areas between adjacent ones of the caps (fig. 3, channel formed by contacts 21a).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 5,926,380) in view of Scherer (US 4,768,077).

Kim discloses all of the elements of the claims in paragraph 3 above, but Kim does not explicitly teach the terminal-bearing element to include a dielectric layer, the terminals and the leads being supported by the dielectric element prior to the assembling step. Scherer teaches a method of forming a lead frame (fig. 4, 40) including a dielectric layer (41), wherein terminals and leads of the frame are supported by the dielectric element prior a step of assembling the lead frame to a semiconductor device (fig. 4; col. 3, lines 41-44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dielectric support layer of Scherer in the lead frame of Kim. One would have been motivated to do this because Scherer taught that the dielectric support layer decreased the probability of breaking the lead frame during manufacturing, thus improving the yield of the manufacturing process of Kim.

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 5,926,380) in view of Salatino et al. (US 5,915,168).

Kim discloses all of the elements of the claims in paragraph 3 above, but Kim does not explicitly teach the plurality of individual spaced-apart active areas (fig. 3, 21) to comprise acoustically-active MEMS devices, the caps covering the active areas associated with the respective acoustically-active MEMS devices. Salatino teaches a method of forming an acoustically-active MEMS device (fig. 2, 242; col. 5, lines 24-33), wherein a plurality of spaced-apart caps (fig. 2, 262; wafer level cap) project upwardly from a main surface of at least a portion of the wafer having a plurality of individual acoustically-active MEMS devices (fig. 3, wafer 202 containing MEMS device 242), each spaced-apart cap covering and protecting a respective MEMS device (fig. 4), the spaced-apart caps defining a plurality of channels (248) between adjacent ones of the active areas and between adjacent ones of the caps, wherein contacts (250) on the wafer are disposed in the channels. Salatino further teaches that external devices are electrically connected to the MEMS device via the contacts (250) disposed in the channels (col. 3, lines 50-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the lead frame assembly method of Kim to form the external electrical connection to the contact pad 250 of Salatino. One would have been motivated to do this because Kim taught that the wafer-level lead frame attachment method reduced the number of fabrication steps, improved device yield and reduced the cost of assembly of the devices compared to conventional methods of attaching individual chips to individual lead frames (Kim, col. 1, lines 52-60 & col. 4, lines 17-28).

Response to Arguments

7. Applicant's arguments with respect to independent claims 1 and 13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hong '040, Lee '540 and Neugebauer '972 disclose methods for wafer-level packaging of semiconductor devices.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN J. FULK whose telephone number is (571)272-8323. The examiner can normally be reached on Monday through Friday, 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Rose can be reached on (571) 272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven J. Fulk/
Examiner, Art Unit 2891